Efabless Chipalooza 2024

Tim Edwards

SVP Analog

efabless

efabless.com

Efabless Caravel

Sky130 open PDK

Chipalooza launch

February 16, 2024

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What is Chipalooza?

“-palooza” from “lollapalooza”:
An extraordinary person or thing
(North American slang)

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Yes, but what is Chipalooza?

The first Efabless challenge event for open-source analog and mixed signal design.

Structured similarly to the AI challenges.

There will be requirements, reviews, deadlines, and awards.

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And why are we running the Chipalooza?

We need to create the next-generation Caravel harness chip.

Everybody talks about AI and Edge IoT and machine learning. There are some very successful SoC products targeting this space.

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And why are we running the Chipalooza?

These applications need to interface to the real world.

That means SoC designers want resources like ADCs, DACs, instrumentation amplifiers, sensors, filters, power monitors, . . .

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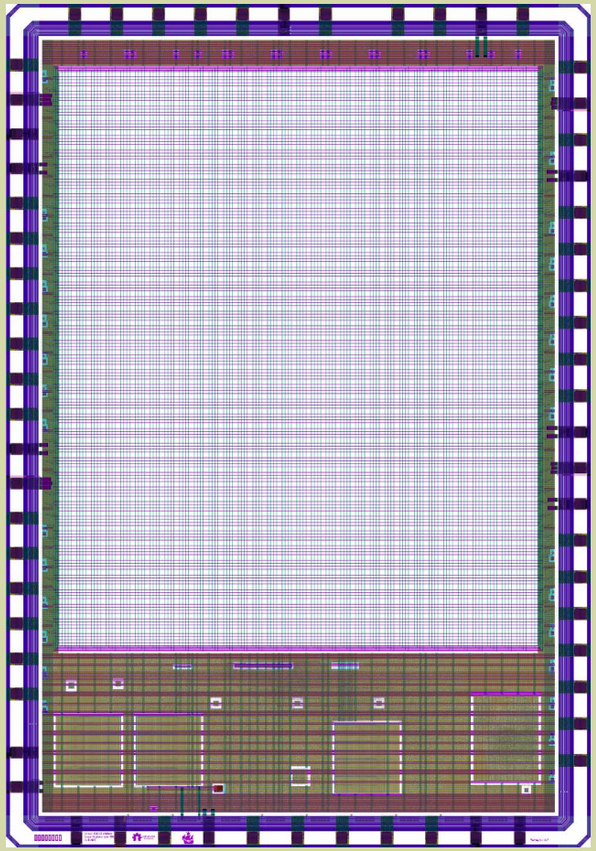
Quick sneak preview of the next-generation Caravel harness chip:



Caravel now

38 GPIOs

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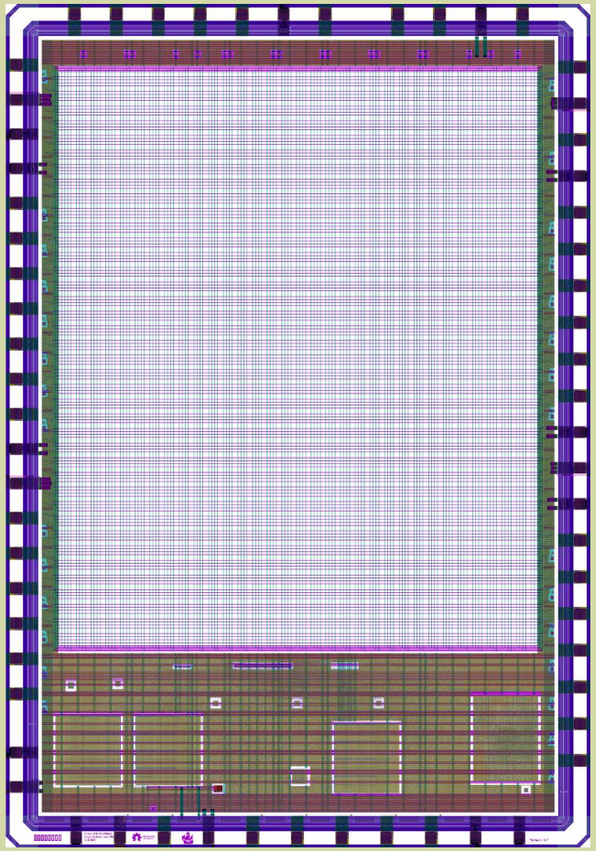
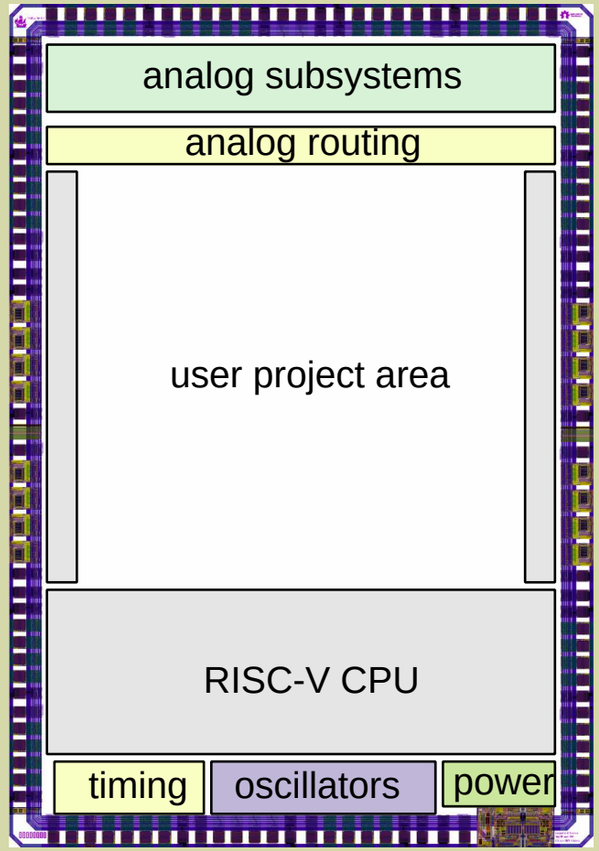
Quick sneak preview of the next-generation Caravel harness chip:



Caravel to be:

66 GPIOs
analog I/O
ADCs
DACs
and lots more!



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And why are we running the Chipalooza?

We want designers to be able to make use of these resources ASAP (realistically, 2025).

We do not have time or staff to develop all of the required analog and mixed-signal IP.

So we're asking our fine (and large!) community of designers to help us out here.

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What do participants get out of Chipalooza?

Designs will be open-sourced and available for other designers for education, reference, re-use, and enhancement.

The best design for each required IP will go on the next-generation Caravel test tapeout on the June chipIgnite shuttle run.

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What do participants get out of Chipalooza?

Designs that make it through the post-layout design review and pass specifications will be integrated into chipIgnite slots and go out on the April chipIgnite shuttle run.

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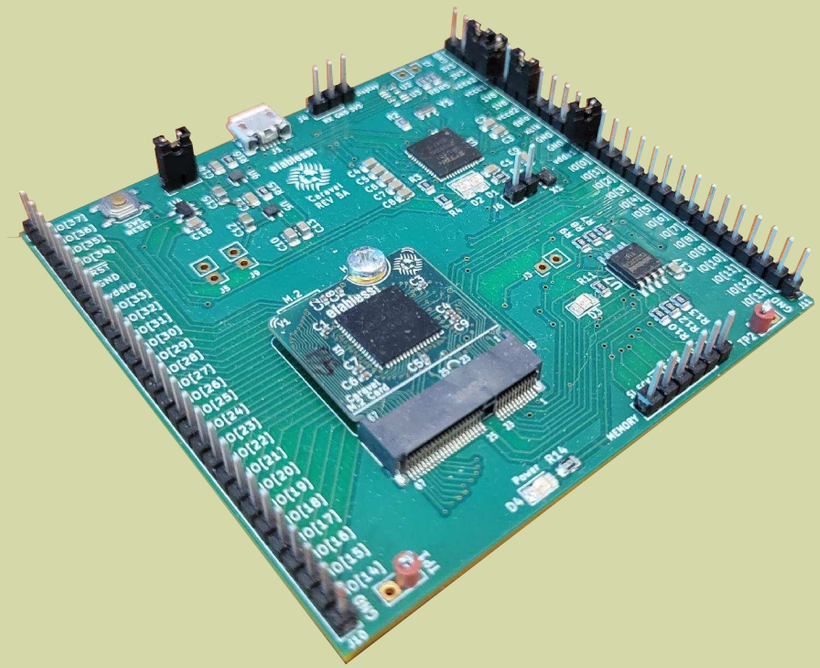
What do participants get out of Chipalooza?

Designers get a development board and assembled parts with their integrated design.



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What do participants get out of Chipalooza?

Awards!

Free Silicon!

and a T-shirt!

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There are rules. Of course there are rules.

Here are the rules:

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1. **Efabless provides a list of the IP blocks that we want, with target specification and pinout.**

See link in:

https://efabless.com/analog-and-mixed-signal-design-challenge

2. Participants will write a proposal.

What block will be designed.

What architecture will be used.

How challenging specs will be met.

Demonstrate feasibility in the sky130 process.

Any departure from specified pinout must be noted (and approved).

3. Proposals will be reviewed and participants selected.

Up to three designers or design teams may be selected for each IP block.

Designers may submit multiple proposals.

The overall goal is to get coverage of all IP needed for the next-generation Caravel.

4. **Designers create a public git repository for the project.**

   The repository must contain all required design files.

   Efabless will specify the filesystem structure of the repository to ensure consistency across IP blocks.

5. **Designers will use open source tools for the design.**

   Open source tools ensure that anybody can re-use the IP.

   Open source tools ensure that all publicly posted files in the design repository are legal.

6. Schematics will be subjected to design review.

Testbenches must be available which simulate all (simulatable) specifications.

All testbench results must meet the specifications.

Any specification that is unreasonable may be reviewed and corrected by agreement with Efabless prior to review.

7. Final layout will be subjected to design review.

Testbenches must simulate all electrical parameters in the spec on parasitic R-C extracted layout.

All testbench results must meet the specifications.

Layouts must be in deep nwell with double guard rings around the entire block.

Layouts must be reasonably compact.

8. **All designs passing all requirements and design reviews will be integrated as standalone circuits on chiplgnite slots on the April 24 shuttle run.**

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There are deadlines.

Please seat yourself before viewing the timeline.

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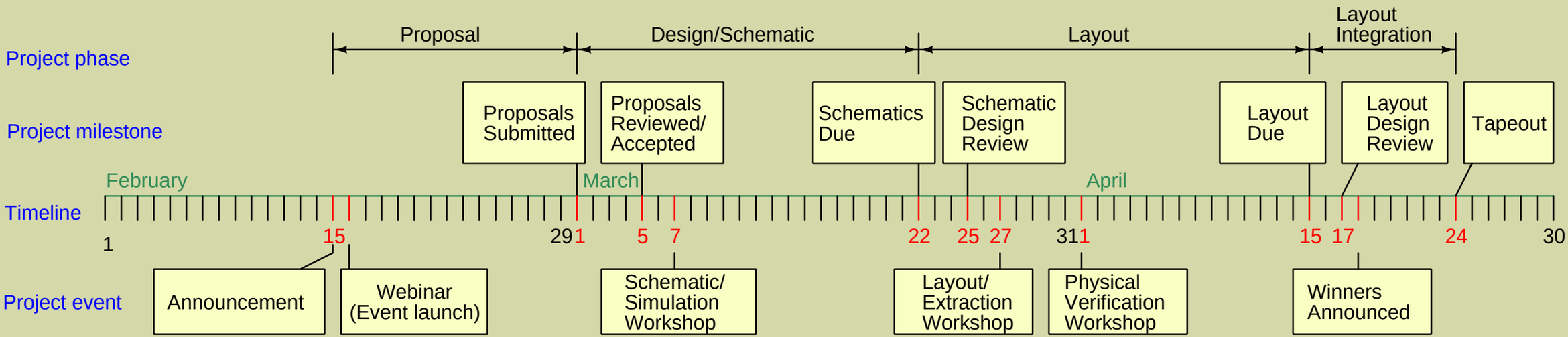
There are deadlines.



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There are deadlines.

		Timeframe	*Total time*
Feb. 16	Challenge Launch	Day 0	Day 0
Mar. 1	Proposals Submitted	14 days	14 days
Mar. 5	Proposals Reviewed/Accepted	4 days	18 days
Mar. 7	Schematic/Simulation Workshop	2 days	20 days
Mar. 22	Schematics Due	15 days	35 days

21 days for schematic design and simulation

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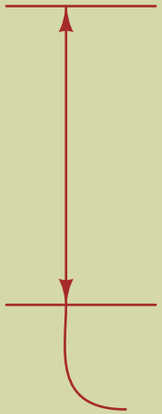
Mar. 7	Schematic/Simulation Workshop	2 days	20 days
Mar. 22	Schematics Due	15 days	35 days
Mar. 25	Schematic Design Review	3 days	38 days
Mar. 27	Layout/Extraction Workshop	2 days	40 days
Apr. 1	Physical Verification Workshop	5 days	45 days
Apr. 15	Layout Due	14 days	59 days



23 days for layout and verification

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Mar. 25	Schematic Design Review	3 days	38 days
Mar. 27	Layout/Extraction Workshop	2 days	40 days
Apr. 1	Physical Verification Workshop	5 days	45 days
Apr. 15	Layout Due	14 days	59 days
Apr. 17	Post-Layout Design Review	2 days	61 days
Apr. 24	Shuttle Run Close Date	7 days	68 days

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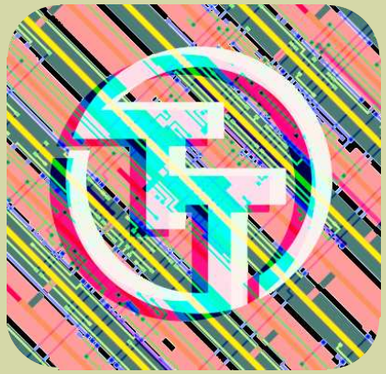
There are awards!

All designs with accepted proposals will get a Tiny Tapeout slot. . . a $300 value.



https://efabless.com/tinytapeout

(Upcoming Tiny Tapeouts will have analog!)

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There are awards!

All designs with accepted proposals will get a Tiny Tapeout slot. . . a $300 value.

All designs which pass the schematic design review and meet specifications will get another Tiny Tapeout slot. . . a $300 value.

https://tinytapeout.com

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There are awards!

All designs with accepted proposals will get a Tiny Tapeout slot. . . a $300 value.

All designs which pass the schematic design review and meet specifications will get another Tiny Tapeout slot. . . a $300 value.

All designs which complete the post-layout design review and meet specifications will get a free 1/4 chipIgnite slot. . . an ~$2500 value.

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Here are the 20 IP blocks you can choose from:

Signal processing

- RDAC, CDAC, IDAC
- ADC
- Rheostat
- Op Amps
- Sallen-Key filter
- Comparators

Sensors

- Temperature sensor

Power management

- Bandgap
- LDO
- POR
- Brownout detector
- Over-voltage detector
- Bias generator

Oscillators

- Crystal oscillators
- PLL

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The spreadsheet has the specs for each block:

Description

Electrical parameters

Pinout

	A	B	C	D	E	F	G
1	**Ultra low-power comparator**						
2							
3	**Description**						
4							
5	Ultra-low power comparator with offset correction						
6							
7	**Parameter**	**Min**	**Typical**	**Max**	**Unit**	**Notes**	
8	Operating Temperature	-40	25	85	°C		
9	Power Consumption (enabled)		2	6	µA	Measured at 1.8V and 25°C	
10	Power Consumption (disabled)		1	2	nA	Measured at 1.8V and 25°C	
11	Input Offset Voltage		1	2	mV	All corners voltage and temperature	
12	Propagation Delay		3	5	µs		
13	Input Common-Mode Range	5	50	95	%	Percent of VDD	
14	Output Current Drive		N/A		µA	(Use standard cell buffer at output)	
15	Output Voltage Swing	0		1.8	V	Rail-to-rail output	
16	Input Capacitance	0.1	0.5	1	pF		
17	Frequency Bandwidth	5	10	20	kHz		
18	PSRR (Power Supply Rejection)	30	40		dB	(negotiable)	
19	CMRR (Common-Mode Rejection)	30	40		dB	(negotiable)	
20	Output load		0.5	1	pF	(condition)	
21							
22							
23	**Pinout**						
24	*Pin name*	*Use*					
25	avdd	analog power		3.3V			
26	dvdd	digital power		1.8V			
27	avss	analog ground					
28	dvss	digital ground					
29	ena	enable		dvdd domain			
30	vinn	negative side input		avdd domain			
31	vinp	positive side input		avdd domain			
32	ibias	bandgap-controlled current bias					
33	vout	output		dvdd domain	CMOS digital		
34							
35							

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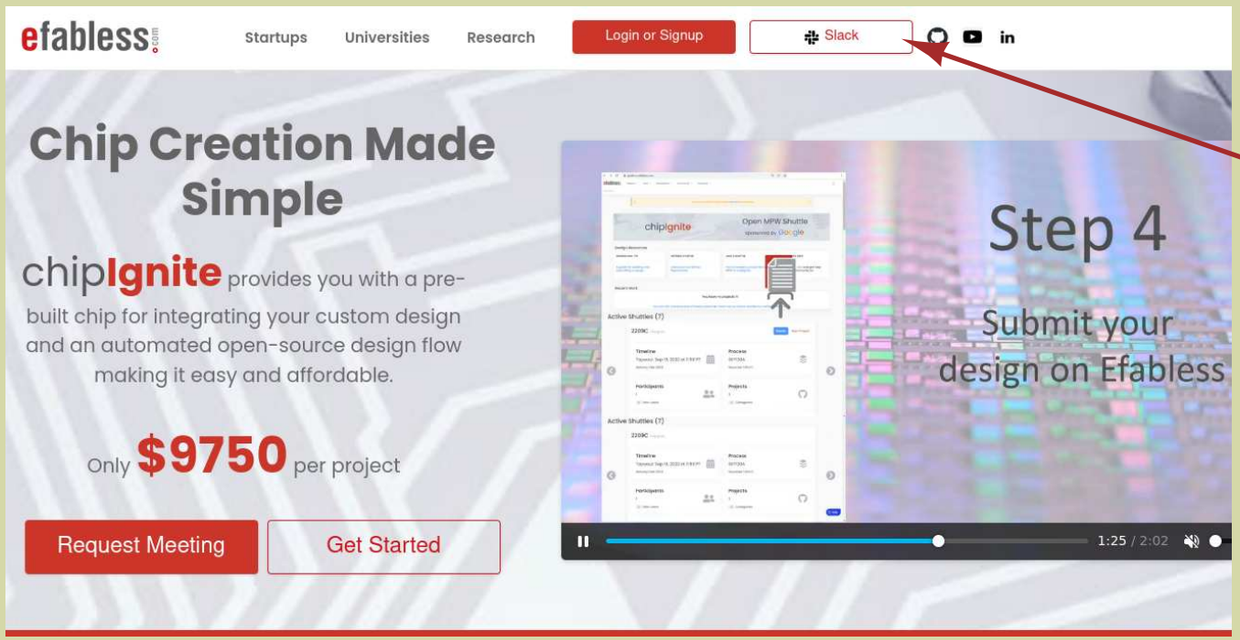
Keep up with the challenge news:

https://www.open-source-silicon.slack.com

New channel #chipalooza



Join from here on
https://efabless.com
if you haven't already.

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Thank you for participating!

Now go start designing!